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Subject: Testing results of the Cayenne Micro Inverter

Dear Mr. Jones

This letter summarizes the testing through February 27, 2013 with the above referenced equipment to the requirements contained in the following standards:

- IEEE Std 1547.1, IEEE Standard Conformance Test Procedures of Equipment Interconnecting Distributed Resources with Electric Power Systems, dated July 1, 2005
- IEEE std C62.41.2, IEEE Recommended Practice on Characterization of Surges in Low-Voltage (1000 V and Less) AC Power Circuits, dated November 11, 2001
- UL 1741, Inverters, converters, controllers and interconnection system equipment for use with distributed energy resources, Second edition, dated January 28, 2010

This testing was authorized by quote 500407519 signed October 22, 2012 and quote 500437258 signed on February 19, 2013.

Currently, all responses to the non-compliances are under evaluation however the testing has completed and all tests were found to be compliant.

Below is the status of the testing for the listing of the Cayenne Micro inverter through March 29, 2013.

Section Number UL 1741	Test Description	Results
42	Maximum - Voltage Measurements	Pass
43	Temperature Test, rated ambient 65°C	Pass
44	Dielectric Voltage-Withstand Test	Pass
45.2	Output Power Characteristics - Output ratings	Pass
45.3	Input Range	Pass
47.2	Abnormal Tests - Output overload test	Pass
47.3	Abnormal Tests - Short-circuit test	Pass
47.4	Abnormal Tests - DC input miswiring test	Pass
47.6	Abnormal Tests - Component Short-and open- circuit	Pass
48	Grounding Impedance Test	Pass
50	Strain Relief Test	Pass
52	Bonding Conductor Test	Pass
61	Rain Test and Sprinkler Tests	Pass

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IEEE 1547	IEEE 1547.1	Per UL 1741 Section 39.1 and 46.1.1 "A utility-interactive inverter or interconnection system equipment (ISE) shall comply with the Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE 1547..."	
Clause		Test	Result
	5.1.2.1	Operational Temperature	Pass
	5.1.2.2	Storage Temperature	Pass
5.1.1	5.2	Response to abnormal voltage	Pass
5.1.1	5.3	Response to abnormal frequency	Pass
5.1.2	5.4	Synchronization	Pass
5.1.3	5.5	<i>-- Interconnect Integrity tests (heading) --</i>	
5.1.3.1	5.5.1	Protection from EMI (IEEE C37.90.2)	Pass
5.1.3.2	5.5.2	Surge withstand (C62.45 and C62.41) Location Category A, B, or C	Pass
5.1.3.3	5.5.3	Paralleling Device	Pass
	5.2	<i>Response to abnormal voltage (Repeat)</i>	Pass
	5.3	<i>Response to abnormal frequency (Repeat)</i>	Pass
	5.4	<i>5.1.2 Synchronization (Repeat)</i>	Pass
5.1.4	5.7	Unintentional Islanding	Pass
4.2.6	5.10	Reconnection to Area EPS	Pass
5.1.5	5.6	Limitation of dc injection	Pass
5.1.6	5.11	Harmonics (current)	Pass
	5.9	Open Phase	Pass
		Sequence for conducting design test per Table 4, IEEE 1547	

If there are any questions regarding the results contained in this report, or any of the other services offered by Intertek, please do not hesitate to contact the undersigned.

Please note, this Letter Report does not represent authorization for the use of any Intertek certification marks.

Completed by:	Matthew Pavloff	Reviewed by:	Tony Dorta
Title:	Project Engineer	Title:	Reviewer
Signature:		Signature	
Date	3/29/2013	Date	3/29/2013